REMARKS

In the above-identified Office Action the five pending claims of the application were rejected on new grounds, wherein the claims were deemed to be obvious in view of the disclosures of the cited Hashimoto, Rashkovskiy, and Shaw patents. In response, independent Claim 30 has been amended in a manner which is believed to provide clear patentable distinctions over that prior art.

In particular, an object of the present invention is to microminiaturize a structure of a color image pickup device, by integrating, in one semiconductor chip, all of an image pickup element, a memory for storing a signal, an interpolation circuit for interpolation of the signal stored, and a signal processing circuit for a color gain adjustment and an another processing. However, in order to achieve this object, it is necessary to overcome the following technical problems:

(a) Conventionally, in case of using a frame memory capable of storing a signal of one frame, a capacity of the memory would be too large to integrate the memory in the one chip together with the other components thereof without degrading a yield ratio and increasing cost.

(b) Conventionally, when an analog signal is converted into a digital signal during processing, different circuit structures are required for processing the analog signal before the conversion and for processing the digital signal after the conversion. Accordingly, the cost of the circuitry is undesirably increased.

According to the present invention, however, not all of the signal in one frame is necessary for interpolating a signal. Instead, it is only necessary that a signal adjacent to the signal to be interpolated is stored in a memory. In order to stress this feature of the present invention, Claim 30 has been amended to required that "the number

of the stored analog image data bits is smaller than the number of the photodetectors included in the image pickup element", and "after a termination of the interpolation for each of the photodetectors of the target basic block unit, in order to perform the interpolation for the next target basic block unit, the block storage circuit performs the storing of the analog image data to replace the analog image data of the basic block units of the photodetectors neighboring the target basic block unit with the analog image data of other basic block units of the photodetectors neighboring the next target basic block unit".

To emphasize the importance of these features, Applicants point out that in the conventional art it is necessary that the frame memory stores several millions of signal bits for the type of image pickup device normally used. In contrast, according to the present invention as disclosed in the Specification, it is only necessary that a basic block unit of 2x2 (4 pixels) store totally 36 bits of signal. Accordingly, the memory can be made significantly compact thereby solving the above problem (a).

Furthermore, according to the present invention, as now set forth in amended Claim 30, a signal processing circuit outputs the analog image data as the output of the color image pickup device. Accordingly, the image pickup device, the memory for storing the signal, an interpolating circuit for interpolating the signal, and a signal processing circuit may be analog circuits, thereby solving the above problem (b).

Moreover, according to the present invention, the image pickup device, the memory for storing the signal, the interpolation circuit for signal interpolating processing, and the signal processing circuit for subjecting the interpolated signal to the processing for

color gain adjustment and another processing are integrated in one semiconductor chip, thereby microminiaturizing the whole structure.

The Prior Art

As pointed out in the Office Action the cited Hashimoto patent is relied upon as disclosing the reading out simultaneously of two horizontal lines of an image signal, and outputting the signal per each color in parallel. However, as also acknowledged in the Office Action, Hashimoto does not disclose any means corresponding to the block storage means and the signal processing circuit of the present invention. With regard to this issue, the Office Action points out that the cited Rashkovskiy patent discloses a digital camera system provided with a memory 18 for storing a signal, and a processor 26 of a computer system for interpolating the pixel signals. However, neither of the Rashkovskiy and Hashimoto references, nor the cited Shaw patent, discloses or suggests the requirements of the present invention, that "the number of the stored analog image data bits is smaller than the number of the photodetectors included in the image pickup element", and "after a termination of the interpolation for each of the photodetectors of the target basic block unit, in order to perform the interpolation for the next target basic block unit, the block storage circuit performs the storing of the analog image data to replace the analog image data of the basic block units of the photodetectors neighboring the target basic block unit with the analog image data of other basic block units of the photodetectors neighboring the next target basic block unit".

Moreover, according to Rashkovskiy, the memory 18 is prepared as a normally used frame memory. Accordingly, the memory 18 is itself a large scale circuit

structure, and it would be substantially impossible to integrate such a large scale frame memory together with the sensor, the interpolation circuit, and the signal processing circuit in one semiconductor chip as in the present invention.

Also, referring to Fig. 10 of the Shaw patent, the element integrated together with the SENSOR array in the one chip is an ADC array. Therefore, it would be apparent that total digital image signal derived from all pixel signals of whole image frame is stored in the frame memory. Accordingly, it would also be substantially impossible to integrate such a large scale frame memory together with the sensor, the interpolation circuit, and the signal processing circuit in one semiconductor chip as in the present invention.

In view of collective deficiencies of the cited Hashimoto, Rashkovskiy, and Shaw patents as rejecting references, Applicants believe that the amended claims are allowable, and the issuance of a Notice of Allowance is solicited.

Applicants' undersigned attorney may be reached in our New York Office by telephone at (212) 218-2100. All correspondence should continue to be directed to our address listed below.

Respectfully submitted,

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